TECHNICAL INFORMATION

HIPERFACE DSL® MASTER IP-Core

SICK
Sensor Intelligence.

This documentation applies to the HIPERFACE DSL® MASTER IP-Core release version 1.07.

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SICK STEGMANN GmbH
Dürrheimer Strasse 36
78166 Donaueschingen, Germany
Tel.: +(49) 771 / 807 – 0
Fax: +(49) 771 / 807 – 100
Internet: www.sick.com
E-mail: info@sick.com

1 Functional description

The HIPERFACE DSL® MASTER IP-Core allows implementing the motor-feedback protocol HIPERFACE DSL® on drives. HIPERFACE DSL® is a fast digital protocol for motor feedback systems that connects servo drives with SICK motor feedback encoders. For details of the protocol, IP-Core details, all implementation and test aspects please see the HIPERFACE DSL® Master Integration Manual (8017595) and HIPERFACE DSL® Master Safety Integration Manual (8017596).

The protocol is implemented in the drive within an FPGA component by the use of this IP-Core. The HIPERFACE DSL® MASTER IP-Core varies according to target FPGA.

The IP-Core comes in two variants for each target FPGA. These variants are to be used in dependence of the safety relevance of the target application:

- “Standard” variants are smaller IP-Cores but do not support safety functions and diagnostics of the protocol and connected motor feedback encoders. When using the “Standard” variants the safety conformance of appropriate SICK motor feedback systems suitable for safety applications can not be claimed.
- “Safe” variants are larger IP-Cores and do support safety functions and diagnostics according to requirements laid out in the HIPERFACE DSL® Master Safety Integration Manual (8017596) and specific motor feedback encoder requirements (see their respective data sheets).

For the host interface two open source interface blocks are delivered as well. These sample interfaces implement either a serial (SPI) or a parallel (EMIFA) interface.

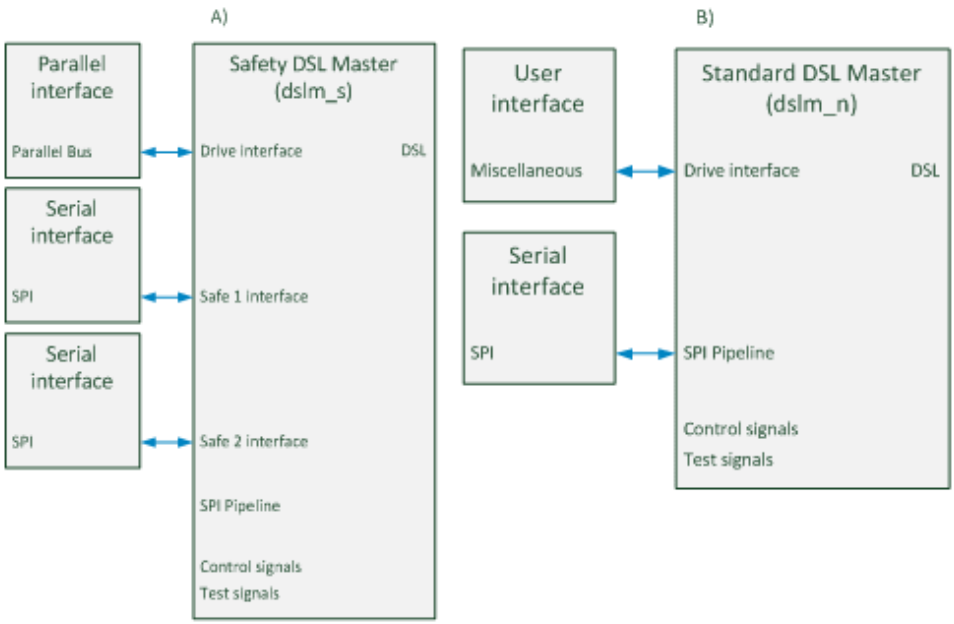

Figure 1: DSL Master Schematic Symbol

A) Safe variant with two parallel interfaces and one serial interface

B) Standard variant with serial interface and User interface

1.1 Features

Support devices	• Xilinx® Spartan-3E • Xilinx® Spartan-6 • Xilinx® Artix 7 • Lattice FPGAs • Altera FPGAs
Variants	• “Standard” for non-safe applications • “Safe” for safety-relevant applications according to SIL2 or SIL3
Host interface options	• User interface • Serial (SPI) • Parallel (EMIFA)

1.2 Technical properties

Table 1: Technical properties HIPERFACE DSL® MASTER IP-Core

Signal specifications	
Design clock – “clk”	
Frequency	75.0 MHz
Frequency tolerance	± 100 ppm
Design reset – “rst”	High-active
Minimum reset duration after power-on/load	20 ns
HIPERFACE DSL® interface – “dsl_out”, “dsl_in”, “dsl_en”	Based on RS-485 specification
Typical signal transmission rate	9’375’000 Baud
Drive Interface	SPI, EMIFA or user defined
Safe 1 Interface (“safety” variant only)	SPI, EMIFA or user defined
Safe 2 Interface (“safety” variant only)	SPI, EMIFA or user defined
SPI-PIPE interface – “spipipe_clk”, “spipipe_miso”, “spipipe_ss” (optional, user-configurable)	Based on SPI specification
Maximum SPI clock	10 MHz
Digital input – “sync”	Drive cycle synchronization
Minimum sync signal duration	40 ns
Maximum sync frequency jitter	2 % based on packet cycle time
Digital output – “interrupt”	User-configurable interrupt, high-active
Digital output – “interrupt_s” (“safety” variant only)	User-configurable interrupt, high-active
Digital output – “link”	DSL link indicator, high-active
Digital input – “bigend”	Register address map selector
Digital output – “fast_pos_rdy”	Position availability indicator
Digital output – “sync_locked”	Drive cycle skew indicator

1.3 FPGA requirements

All FPGA types	
Timing constraints (clk)	13 ns period
Xilinx® Artix 7	
Number of Slice Registers	2,340 (standard variant, serial interface) 2,739 (safe variant, 3x serial)
Altera FPGAs	
Logic Elements	3,634 (standard variant, serial, interface) 4,698 (safe variant, 3x serial)
Lattice FPGAs	
Logic Elements	3,896 (standard variant, serial interface) 4,462 (safe variant, 3x serial)

1.4 Scope of delivery

The supplied Software contains the following files:

- Documentation:
  - Technical Information 8025710
  - HIPERFACE DSL® MASTER Integration Manual
- IP-Core:
  - Xilinx Spartan-3E variants as NGC IP-core
  - Xilinx Spartan-6 variants as NGC IP-core
  - Altera variants as encrypted VHDL project (for any FPGA type)

1.5 Order Information

Please note that the software is delivered via MySick.

Type	Part no.
HIPERFACE DSL® MASTER IP-Core	1614697

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Australia
Phone +61 (3) 9457 0600
1800 33 48 02 – tollfree
E-Mail sales@sick.com.au

Austria
Phone +43 (0) 2236 62288-0
E-Mail office@sick.at

Belgium/Luxembourg
Phone +32 (0) 2 466 55 66
E-Mail info@sick.be

Brazil
Phone +55 11 3215-4900
E-Mail comercial@sick.com.br

Canada
Phone +1 905.771.1444
E-Mail cs.canada@sick.com

Czech Republic
Phone +420 2 57 91 18 50
E-Mail sick@sick.cz

Chile
Phone +56 (2) 2274 7430
E-Mail chile@sick.com

China
Phone +86 20 2882 3600
E-Mail info.china@sick.net.cn

Denmark
Phone +45 45 82 64 00
E-Mail sick@sick.dk

Finland
Phone +358-9-25 15 800
E-Mail sick@sick.fi

France
Phone +33 1 64 62 35 00
E-Mail info@sick.fr

Germany
Phone +49 (0) 2 11 53 01
E-Mail info@sick.de

Hong Kong
Phone +852 2153 6300
E-Mail ghk@sick.com.hk

Hungary
Phone +36 1 371 2680
E-Mail ertekesites@sick.hu

India
Phone +91-22-6119 8900
E-Mail info@sick-india.com

Israel
Phone +972-4-6881000
E-Mail info@sick-sensors.com

Italy
Phone +39 02 27 43 41
E-Mail info@sick.it

Japan
Phone +81 3 5309 2112
E-Mail support@sick.jp

Malaysia
Phone +603-8080 7425
E-Mail enquiry.my@sick.com

Mexico
Phone +52 (472) 748 9451
E-Mail mario.garcia@sick.com

Netherlands
Phone +31 (0) 30 229 25 44
E-Mail info@sick.nl

New Zealand
Phone +64 9 415 0459
0800 222 278 – tollfree
E-Mail sales@sick.co.nz

Norway
Phone +47 67 81 50 00
E-Mail sick@sick.no

Poland
Phone +48 22 539 41 00
E-Mail info@sick.pl

Romania
Phone +40 356-17 11 20
E-Mail office@sick.ro

Russia
Phone +7 495 283 09 90
E-Mail info@sick.ru

Singapore
Phone +65 6744 3732
E-Mail sales.gsg@sick.com

Slovakia
Phone +421 482 901 201
E-Mail mail@sick-sk.sk

Slovenia
Phone +386 591 78849
E-Mail office@sick.si

South Africa
Phone +27 (0)11 472 3733
E-Mail info@sickautomation.co.za

South Korea
Phone +82 2 786 6321
E-Mail info@sickkorea.net

Spain
Phone +34 93 480 31 00
E-Mail info@sick.es

Sweden
Phone +46 10 110 10 00
E-Mail info@sick.se

Switzerland
Phone +41 41 619 29 39
E-Mail contact@sick.ch

Taiwan
Phone +886-2-2375-6288
E-Mail sales@sick.com.tw

Thailand
Phone +66 2 645 0009
E-Mail marcom.th@sick.com

Turkey
Phone +90 (216) 528 50 00
E-Mail info@sick.com.tr

United Arab Emirates
Phone +971 (0) 4 88 65 878
E-Mail info@sick.ae

United Kingdom
Phone +44 (0)17278 31121
E-Mail info@sick.co.uk

USA
Phone +1 800.325.7425
E-Mail info@sick.com

Vietnam
Phone +65 6744 3732
E-Mail sales.gsg@sick.com

Further locations at **www.sick.com**

SICK AG | Waldkirch | Germany | www.sick.com

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